

TSMC-03-485



April 9, 2004

To: Commissioner for Patents  
P.O.Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/780,513 02/17/04 |  
Bor-Wen Chan et al.  
A METHOD TO FORM A METAL SILICIDE  
GATE DEVICE  
| \_\_\_\_\_ |

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
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P.O. Box 1450, Alexandria, VA 22313-1450, on April 12, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 4/12/04

TSMC-03-485

U.S. Patent 6,465,309 to Xiang et al., "Silicide Gate Transistors," describes a method to form a silicide gate transistor.

U.S. Patent 6,475,908 to Lin et al., "Dual Metal Gate Process: Metals and Their Silicides," describes a method to form metal silicide gate MOS transistors.

U.S. Patent 6,528,402 to Tseng, "Dual Salicidation Process," describes a method to form a self-aligned, silicide gate.

Sincerely,

A handwritten signature in black ink, appearing to be 'SBA', written over a horizontal line.

Stephen B. Ackerman,  
Reg. No. 37761

APR 15 2004

(Use several sheets if necessary)

License Number

10/780, 513

Bor-Wen Chan et al.

02/17/04

Group Art Unit

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~~NOTED~~

[illegible]


DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.